WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, the method comprising:

forming an opening in a dielectric layer, comprising a low-k material having a pendant functional group, overlying a lower conductive feature, the opening defined by sidewalls of the low-k dielectric layer;

depositing a sealant layer of dielectric material on the sidewalls of the dielectric layer, the dielectric material having a functional group which bonds to the pendant functional group of the low-k material;

depositing a barrier metal layer lining the opening and on the sealant layer; and

filling the opening with a conductive material, wherein

the sealant layer prevents the barrier metal or a precursor used to deposit the barrier metal from penetrating the low-k material.

2. The method according to claim 1, comprising:

forming the opening as a dual damascene opening;

depositing a Ta and/or TaN barrier metal layer by CVD or ALD;

filling the opening with copper (Cu) or a Cu alloy as the conductive material;

planarizing by chemical-mechanical polishing such that an upper surface of the Cu or Cu alloy is substantially coplanar with an upper surface of the low-k dielectric layer; and

depositing a capping layer.

3. The method according to claim 1, wherein the low-k material is a porous organosilicate.

4. The method according to claim 3, wherein the pendant functional group comprises a silanol.

5. The method according to claim 4, comprising depositing a dielectric material having a silylating functional group as the sealant layer.

6. The method according to claim 5, comprising depositing a conformal, heat stable polymer as the sealant layer.

7. The method according to claim 6, comprising depositing a layer of a siloxane polymer as the sealant layer.

8. The method according to claim 1, comprising depositing a heat stable, conformable dielectric material comprising a polymer having a polymeric chain with the functional group at ends of the chain as the sealant layer.

9. The method according to claim 1, wherein the low-k material is a porous material comprising pores with a diameter of about 10Å to about 100Å.

10. The method according to claim 9, wherein the pores are interconnected.

11. The method according to claim 1, comprising depositing the sealant layer at a thickness of about 10Å to about 100Å.

12. A semiconductor device comprising:

an interlayer dielectric (ILD), comprising a low-k material having a pendant functional group, overlying a lower conductive feature;

an opening in the ILD overlying the lower conductive feature, the opening defined by sidewalls of the low-k material;

a sealant layer on the side surfaces of the low-k material, the sealant layer comprising a dielectric material having a functional group bonded to the pendant functional group of the low-k material;

a barrier metal layer lining the opening and on the sealant layer; and

a conductive material filling the opening.

13. The semiconductor device according to claim 12, wherein:

the opening is a dual damascene opening;

the barrier metal layer comprises Ta and/or TaN;

the conductive material is copper (Cu) or a Cu alloy; and

a capping layer is on an upper surface of the Cu or Cu alloy.

14. The semiconductor device according to claim 12, wherein the sealant layer is a heat stable, conformal layer having a thickness of about 10Å to about 100Å.

15. The semiconductor device according to claim 12, wherein the low-k material is a porous material comprising pores having a diameter of about 10Å to about 100Å.

16. The semiconductor device according to claim 15, wherein the pores are interconnected.

17. The semiconductor device according to claim 12, wherein the low-k material comprises a porous organosilicate.

18. The semiconductor device according to claim 17, wherein the sealant layer comprises a siloxane polymer.

19. The semiconductor device according to claim 18, wherein the siloxane polymer comprises a silylating functional group bonded to a pendant silanol functional group on the organosilicate.